REMARKS

Entry of this Amendment in accordance with the provisions of 37 CFR § 1.114 is respectfully requested.

This Amendment is in response to the Final Office Action dated May 12, 2004. It is noted that the present Amendment is being filed as a Submission with Request for Continued Examination (RCE) being filed herewith.

At the outset, appreciation is expressed to the Examiner for the indication of allowable subject matter in claim 27. By the present Amendment, claim 27 has been amended to clarify the language thereof in response to the 35 U.S.C. § 112, second paragraph, rejection set forth on page 4 of the Final Office Action. In particular, clear antecedent basis has been provided for the language of claim 27 by virtue of the clarification that each group includes centrally emitter electrodes located between first and second end emitter electrodes. Therefore, reconsideration and removal of the 35 U.S.C. § 112, second paragraph, rejection regarding claim 27, and allowance of claim 27 is respectfully requested.

In addition, by the present Amendment, claim 26 has also been amended to clarify the language thereof. In particular, the negative limitation objected to in the Final Office Action has been removed, and claim 26 has been redrafted to define the location of the first and second end electrodes in a manner similar to that set forth in claim 27. More specifically, the location of these first and second end emitter electrodes has been defined as being at opposite ends of the emitter electrodes in the central area of the group to protrude from the areas which the through holes in the wiring board occupy. It is respectfully submitted that clear support exists for this language in the specification (for example, by virtue of the illustrations provided in

Fig. 8 and the discussion thereof on page 23, line 5 et seq. regarding the fact that the thermal vias in the multilayer wiring board are not arranged below the emitter electrodes nearest to the ends of the semiconductor substrate). Therefore, entry of this Amendment and removal of the 35 U.S.C. § 112, first and second paragraph, rejections, together with the allowance of claim 26, is respectfully requested.

Also by the present Amendment, minor clarifying amendments have been made to claims 14 and 23, and new claims 28-49 have been added to further define features of the present invention, as will be discussed below.

In addition, by the present Amendment, a Substitute Specification is provided which includes an amendment to define the elements 10A and 10B shown in the drawings, and to indicate that Figs. 3, 4, 10 and 11 are prior art. Accordingly, reconsideration and removal of the objections to the drawings directed to these points on page 2 of the Final Office Action is respectfully requested.

Reconsideration and removal of the rejection to claims 14-23 as being anticipated by Shirakawa (EP 1077494) is respectfully requested. In the Final Office Action, it is stated that Shirakawa meets the limitations of these claims because Shirakawa discloses:

> "A multilayer wiring board 12, 13 having through holes 10b in a thickness-wise direction, wherein a semiconductor substrate 1 mounted on the multilayer wiring board has through holes 10 in a thickness-wise direction thereof."

With regard to this, it is noted that this reading of Shirakawa is intended to cover the present claims 14-23, all of which specifically define an arrangement wherein a semiconductor substrate is mounted on a multilayer wiring board which has one or more through holes in a cross plane or a thickness-wise direction.

Turning to the actual Shirakawa reference, it is respectfully submitted that the elements pointed out in the Final Office Action in Shirakawa as presumably reading on the present claims are not, in fact, actually the elements stated in the Final Office Action. More specifically, the Final Office Action begins by defining a multilayer wiring board in Shirakawa as the numerals 12 and 13. However, referring to paragraph 50 in column 10 of Shirakawa, it is clearly set forth that the numeral 13 identifies a substrate and the numeral 12 identifies a plated heat sink layer for the substrate. This is specifically defined in Shirakawa in column 10, line 33 et seq. as:

> "A semi-insulating GaAs substrate 13, as well as a plated heat sink layer (hereinafter, referred to as "PHS layer") 12 made of metal and provided on a rear surface of the substrate 13."

As such, it is quite clear that the numerals 12 and 13 of Shirakawa actually simply refer to a substrate with a plated heat sink layer, and not to a multilayer wiring board. As such, the elements 12 and 13 of Shirakawa, identified by Shirakawa as a plated heat sink and a substrate, correspond to the elements 1 and 6 of the present drawings, noting that the element 1 identified the substrate and the element 6 identifies the plated heat sink thereon. This is very different than the multilayer wiring board, identified in the present drawings with the numeral 3, which the substrate with its plated heat sink is shown as mounted upon in the drawings of the present application.

The Final Office Action goes on to state on page 5 that the substrate in Shirakawa is identified with the numeral 1. However, as noted above, the numeral 13 is actually used in Shirakawa to denote a substrate. The numeral 1, on the other hand, is identified as "an emitter layer", as clearly set forth in column 10, line 30.

As a result, it is quite clear that there is no corollary for the claimed multilayer wiring board in Shirakawa. Quite to the contrary, Shirakawa merely discloses a substrate with a plated heat sink on the rear surface thereof, similar to that of the prior art shown in Fig. 10 of the present application. Accordingly, Shirakawa merely discloses a portion of the present claims, and completely lacks the claimed relationship between the substrate and the multilayer wiring board on which it is mounted. Therefore, reconsideration and allowance of claims 14-23, each of which specifically defines the relationship between the semiconductor substrate and the multilayer wiring board, is respectfully requested.

With regard to this, reconsideration and allowance of newly presented claims 28-49 is also respectfully requested. These dependent claims add the feature to each of the claims 14-23, as well as claims 25 and 26, of the plated heat sink being located on the second main surface of the semiconductor substrate. This even further distinguishes over Shirakawa because, in reading Shirakawa on these claims, the element 12 of Shirakawa reads on the plated heat sink of claims 28-49 while the claim substrate reads on the numeral 13 of Shirakawa. As such, there are no other corresponding elements in Shirakawa which could possibly construed as the multilayer wiring board. On the other hand, if an attempt is made to read the claimed multilayer wiring board on the elements 12 and 13, there are no elements left to read on the claimed substrate with the plated heat sink. Accordingly, reconsideration and allowance of these new dependent claims 28-49 is also respectfully requested.

Reconsideration and allowance of independent claim 24 is also respectfully requested. In the Final Office Action, this claim has been rejected as being

anticipated over Applicants' admitted prior art. Regarding this, reference is made to pages 12-22 of the specification.

At the outset, it is noted that pages 12-22 are not all directed to admitted prior art. In particular some portion so of pages 12-22 discuss prior art and other portions describe embodiments of the present invention. For example, beginning on page 16, line 26 et seq., a description begins of the embodiments of the present invention, beginning with Figs. 1 and 2. Therefore, it is respectfully submitted that it is improper to use those portions of which the disclosure from page 16, line 26 et seq. through page 22 as prior art are, in fact, directed to embodiments of the present invention rather than the prior art.

Beyond this, it is respectfully submitted that the prior art which is described on pages 12-16 of the specification referring to Figs. 10 and 11 fail to teach or suggest the feature set forth in independent claim 24. These pages 12-16 describe a conventional structure of a hetero-bipolar transistor arrangement formed on a semiconductor substrate 14 with the alignment of the rows constituting a comb-type finger electrode arrangement and through holes 5. Page 19, line 24 through page 20, line 8 describes Figs. 3 and 4 in terms of another conventional prior art arrangement of an alignment of a semiconductor substrate and a wiring board 3. However, contrary to the present claimed invention, in these prior art arrangements, in the row constituted as emitter electrodes 7 and via holes 5 the via holes in the adjacent rows are arranged at the same position, and the adjacent rows are also arranged at the same position on the semiconductor substrate. As such, this admitted prior art fails to provide any teaching regarding the positional shifting of the via holes from one another among adjacent row, or the positional shifting of the

adjacent rows themselves from one another. Therefore, it is respectfully submitted that claim 24 clearly defines over the admitted prior art, and reconsideration and removal of this ground of rejection is respectfully requested.

As a final note, appreciation is expressed for the indication of the allowance of claim 25. Since this claim is in dependent format, it has been rewritten as an independent claim incorporating the subject matter of its parent claim 24. Therefore, allowance of claim 25 is respectfully requested.

If the Examiner believes that there are any matters which can be resolved by way of either a telephone or a personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus,

LLP Deposit Account No. 01-2135 (Docket No. 500.40530X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dlt

1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Telephone: (703) 312-6600
Facsimile: (703) 312-6666

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Figs. 3, 4, 10 and 11. These sheets replace the original sheets showing Figs. 3, 4, 10 and 11. Each of Figs. 3, 4, 10 and 11 has been labeled as prior art, in response to the requirement to do so in the May 12, 2004 Final Office Action.

FIG.3
(PRIOR ART)

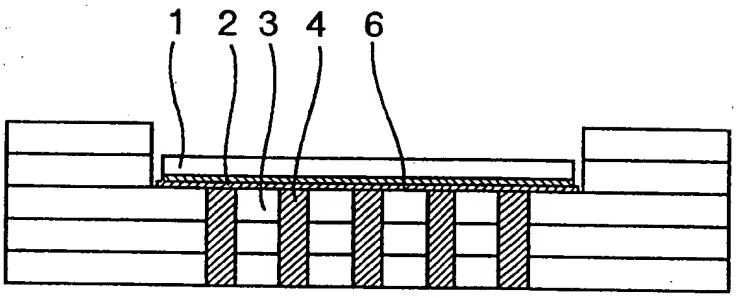

FIG.4
(PRIOR ART)

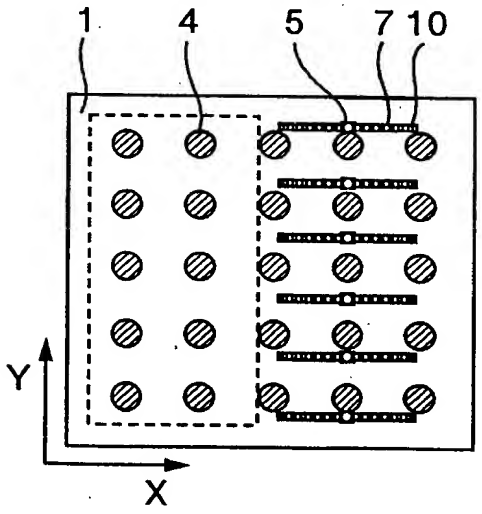

FIG.10
(PRIOR ART)

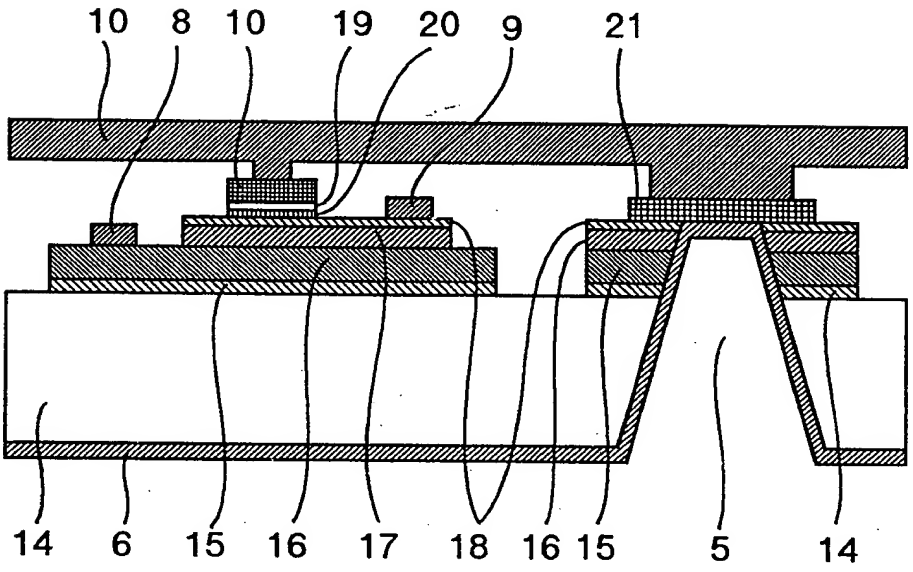

FIG.11
(PRIOR ART)